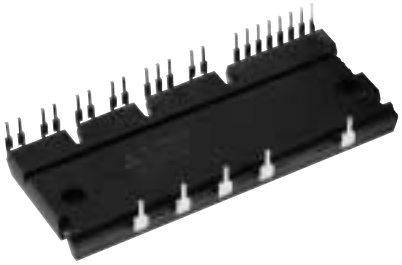
# PS21865/-A

**TRANSFER-MOLD TYPE**
**INSULATED TYPE**

## PS21865



### INTEGRATED POWER FUNCTIONS

600V/20A low-loss 5th generation IGBT inverter bridge for 3 phase DC-to-AC power conversion

### INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

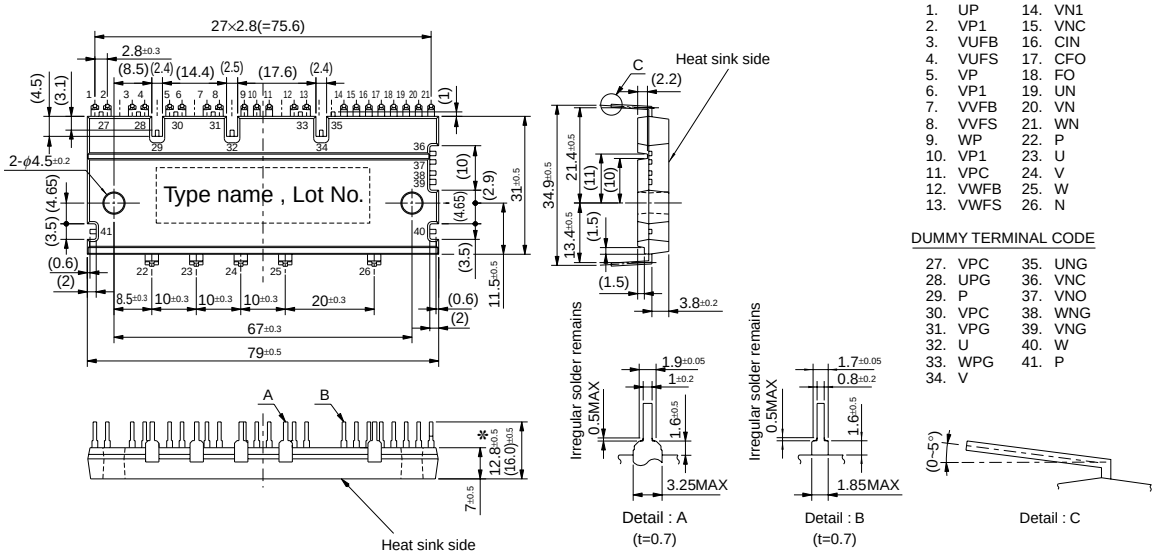
- For upper-leg IGBTs : Drive circuit, High voltage isolated high-speed level shifting, Control supply under-voltage (UV) protection.
- For lower-leg IGBTs : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC). (Fig.3)
- Fault signaling : Corresponding to an SC fault (Lower-side IGBT) or a UV fault (Lower-side supply).
- Input interface : 5V line CMOS/TTL compatible. (High Active)
- UL Approved : Yellow Card No. E80276

## APPLICATION

AC100V~200V three-phase inverter drive for small power motor control.

**Fig. 1 PACKAGE OUTLINES**

Dimensions in mm




TERMINAL CODE

| | | | |
|---|---|---|---|
| 1. | UP | 14. | VN1 |
| 2. | VP1 | 15. | VNC |
| 3. | VUFB | 16. | CIN |
| 4. | VUFS | 17. | CFO |
| 5. | VP | 18. | FO |
| 6. | VP1 | 19. | UN |
| 7. | VVFB | 20. | VN |
| 8. | VVFS | 21. | WN |
| 9. | WP | 22. | P |
| 10. | VP1 | 23. | U |
| 11. | VPC | 24. | V |
| 12. | VWFB | 25. | W |
| 13. | VWFS | 26. | N |

DUMMY TERMINAL CODE

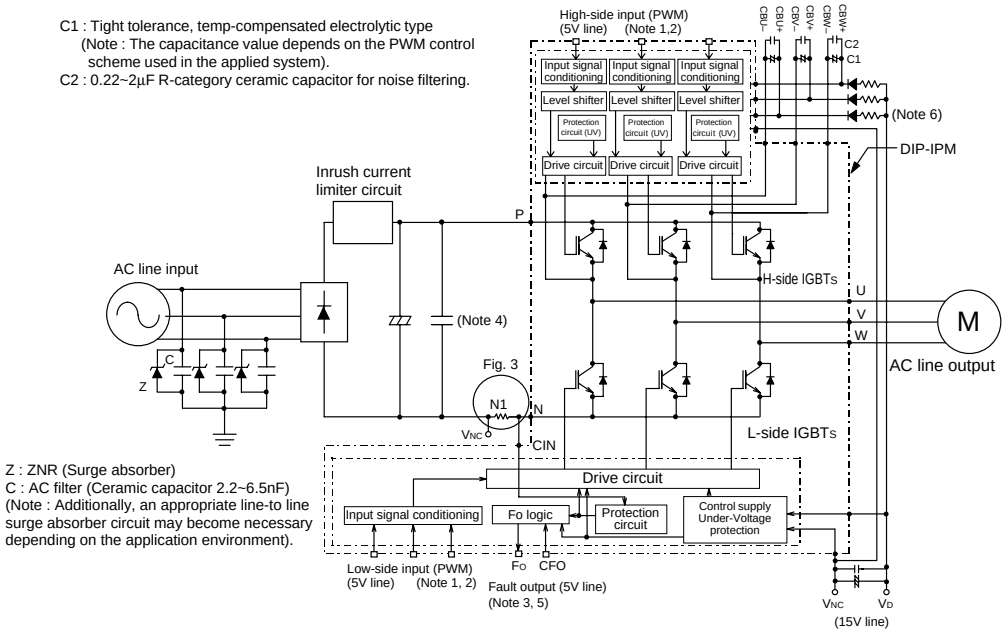
| | | | |
|---|---|---|---|
| 27. | VPC | 35. | UNG |
| 28. | UPG | 36. | VNC |
| 29. | P | 37. | VNO |
| 30. | VPC | 38. | WNG |
| 31. | VPG | 39. | VNG |
| 32. | U | 40. | W |
| 33. | WPG | 41. | P |
| 34. | V | | |

✻ -A : Long terminal type (16.0mm)



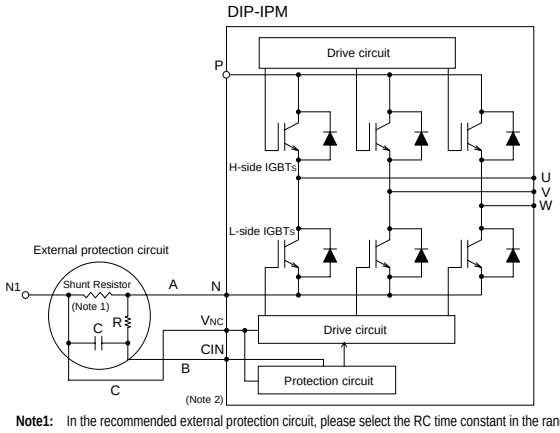
MITSUBISHI ELECTRIC

## Fig. 2 INTERNAL FUNCTIONS BLOCK DIAGRAM (TYPICAL APPLICATION EXAMPLE)

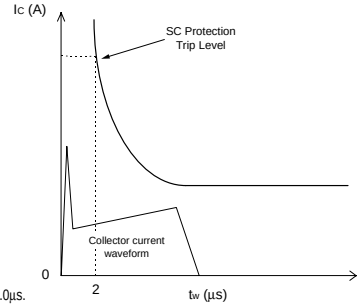



**Note1:** Input logic is high-active. There is a 2.5kΩ (min) pull-down resistor built-in each input circuit. When using an external CR filter, please make it satisfy the input threshold voltage.
**2:** By virtue of integrating an application specific type HVIC inside the module, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible. (see also Fig. 8)
**3:** This output is open collector type. The signal line should be pulled up to the positive side of the 5V power supply with approximately 10kΩ resistance. (see also Fig. 8)
**4:** The wiring between the power DC link capacitor and the PN1 terminals should be as short as possible to protect the DIP-IPM against catastrophic high surge voltages. For extra precaution, a small film type snubber capacitor (0.1~0.22µF, high voltage type) is recommended to be mounted close to these PN1 DC power input pins.
**5:** Fo output pulse width should be decided by putting external capacitor between CFO and $V_{NC}$ terminals. (Example : CFO=22nF → $t_{FO}$=1.8ms (Typ.))
**6:** High voltage (600V or more) and fast recovery type (less than 100ns) diodes should be used in the bootstrap circuit.

## Fig. 3 EXTERNAL PART OF THE DIP-IPM PROTECTION CIRCUIT




Short Circuit Protective Function (SC) :
SC protection is achieved by sensing the L-side DC-Bus current (through the external shunt resistor) after allowing a suitable filtering time (defined by the RC circuit).
When the sensed shunt voltage exceeds the SC trip-level, all the L-side IGBTs are turned OFF and a fault signal (Fo) is output. Since the SC fault may be repetitive, it is recommended to stop the system when the Fo signal is received and check the fault.




**Note1:** In the recommended external protection circuit, please select the RC time constant in the range 1.5~2.0µs.
**2:** To prevent erroneous protection operation, the wiring of A, B, C should be as short as possible.

**MAXIMUM RATINGS** ($T_j$ = 25°C, unless otherwise noted)

**INVERTER PART**

| Symbol | Parameter | Condition | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Applied between P-N | 450 | V |
| $V_{CC(surge)}$ | Supply voltage (surge) | Applied between P-N | 500 | V |
| $V_{CES}$ | Collector-emitter voltage | | 600 | V |
| ±$I_C$ | Each IGBT collector current | $T_f$ = 25°C | 20 | A |
| ±$I_{CP}$ | Each IGBT collector current (peak) | $T_f$ = 25°C, less than 1ms | 40 | A |
| $P_C$ | Collector dissipation | $T_f$ = 25°C, per 1 chip | 52.6 | W |
| $T_j$ | Junction temperature | (Note 1) | –20~+125 | °C |

**Note 1** : The maximum junction temperature rating of the power chips integrated within the DIP-IPM is 150°C (@ $T_f \leq$ 100°C) however, to ensure safe operation of the DIP-IPM, the average junction temperature should be limited to $T_{j(ave)} \leq$ 125°C (@ $T_f \leq$ 100°C).

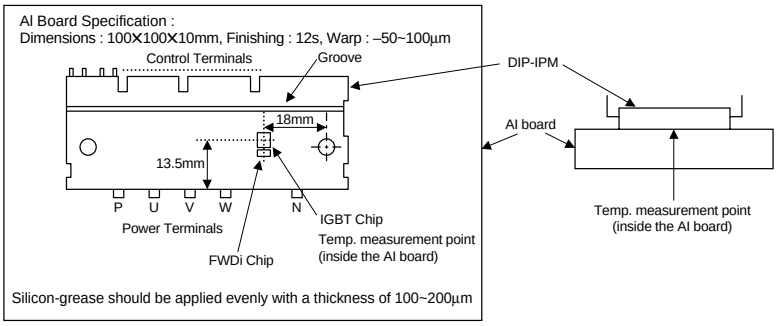
**CONTROL (PROTECTION) PART**

| Symbol | Parameter | Condition | Ratings | Unit |
|---|---|---|---|---|
| $V_D$ | Control supply voltage | Applied between $V_{P1}$-$V_{PC}$, $V_{N1}$-$V_{NC}$ | 20 | V |
| $V_{DB}$ | Control supply voltage | Applied between $V_{UFB}$-$V_{UFS}$, $V_{VFB}$-$V_{VFS}$, $V_{WFB}$-$V_{WFS}$ | 20 | V |
| $V_{IN}$ | Input voltage | Applied between $U_P$, $V_P$, $W_P$-$V_{PC}$, $U_N$, $V_N$, $W_N$-$V_{NC}$ | –0.5~$V_D$+0.5 | V |
| $V_{FO}$ | Fault output supply voltage | Applied between $F_O$-$V_{NC}$ | –0.5~$V_D$+0.5 | V |
| $I_{FO}$ | Fault output current | Sink current at $F_O$ terminal | 1 | mA |
| $V_{SC}$ | Current sensing input voltage | Applied between CIN-$V_{NC}$ | –0.5~$V_D$+0.5 | V |

**TOTAL SYSTEM**

| Symbol | Parameter | Condition | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC(PROT)}$ | Self protection supply voltage limit (short circuit protection capability) | $V_D$ = 13.5~16.5V, Inverter part<br>$T_j$ = 125°C, non-repetitive, less than 2 µs | 400 | V |
| $T_f$ | Module case operation temperature | (Note 2) | –20~+100 | °C |
| $T_{stg}$ | Storage temperature | | –40~+125 | °C |
| $V_{iso}$ | Isolation voltage | 60Hz, Sinusoidal, AC 1 minute, connection pins to heat-sink plate | 2500 | $V_{rms}$ |

**Note 2 : $T_f$ MEASUREMENT POINT**



## THERMAL RESISTANCE

| Symbol | Parameter | Condition | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $R_{th(j-f)Q}$ | Junction to case thermal resistance (Note 3) | Inverter IGBT part (per 1/6 module) | — | — | 1.90 | °C/W |
| $R_{th(j-f)F}$ | | Inverter FWDi part (per 1/6 module) | — | — | 3.00 | °C/W |

**Note 3:** Grease with good thermal conductivity should be applied evenly with about +100μm~+200μm on the contacting surface of DIP-IPM and heat-sink.

## ELECTRICAL CHARACTERISTICS ($T_j$ = 25°C, unless otherwise noted)

### INVERTER PART

| Symbol | Parameter | Condition | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | $V_D = V_{DB}$ = 15V, $V_{IN}$ = 5V | $I_C$ = 20A, $T_j$ = 25°C | — | 1.60 | 2.10 | V |
| | | | $I_C$ = 20A, $T_j$ = 125°C | — | 1.70 | 2.20 | |
| $V_{EC}$ | FWDi forward voltage | $T_j$ = 25°C, $-I_C$ = 20A, $V_{IN}$ = 0V | | — | 1.50 | 2.00 | V |
| $t_{on}$ | Switching times | $V_{CC}$ = 300V, $V_D = V_{DB}$ = 15V, $I_C$ = 20A, $T_j$ = 125°C, $V_{IN}$ = 0 ↔ 5V, Inductive load (upper-lower arm) | | 0.70 | 1.30 | 1.90 | μs |
| $t_{rr}$ | | | | — | 0.30 | — | μs |
| $t_{c(on)}$ | | | | — | 0.40 | 0.60 | μs |
| $t_{off}$ | | | | — | 1.60 | 2.20 | μs |
| $t_{c(off)}$ | | | | — | 0.50 | 0.80 | μs |
| $I_{CES}$ | Collector-emitter cut-off current | $V_{CE} = V_{CES}$ | $T_j$ = 25°C | — | — | 1 | mA |
| | | | $T_j$ = 125°C | — | — | 10 | |

### CONTROL (PROTECTION) PART

| Symbol | Parameter | Condition | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $I_D$ | Circuit current | $V_D = V_{DB}$ = 15V, $V_{IN}$ = 5V | Total of $V_{P1}$-$V_{PC}$, $V_{N1}$-$V_{NC}$ | — | — | 5.00 | mA |
| | | | $V_{UFB}$-$V_{UFS}$, $V_{VFB}$-$V_{VFS}$, $V_{WFB}$-$V_{WFS}$ | — | — | 0.40 | mA |
| | | $V_D = V_{DB}$ = 15V, $V_{IN}$ = 0V | Total of $V_{P1}$-$V_{PC}$, $V_{N1}$-$V_{NC}$ | — | — | 7.00 | mA |
| | | | $V_{UFB}$-$V_{UFS}$, $V_{VFB}$-$V_{VFS}$, $V_{WFB}$-$V_{WFS}$ | — | — | 0.55 | mA |
| $V_{FOH}$ | Fault output voltage | $V_{SC}$ = 0V, $F_O$ circuit pull-up to 5V with 10kΩ | | 4.9 | — | — | V |
| $V_{FOL}$ | | $V_{SC}$ = 1V, $I_{FO}$ = 1mA | | — | — | 0.95 | V |
| $V_{SC(ref)}$ | Short circuit trip level | $T_j$ = 25°C, $V_D$ = 15V (Note 4) | | 0.43 | 0.48 | 0.53 | V |
| $I_{IN}$ | Input current | $V_{IN}$ = 5V | | 1.0 | 1.5 | 2.0 | mA |
| $UV_{DBt}$ | Supply circuit under-voltage protection | $T_j \leq$ 125°C | Trip level | 10.0 | — | 12.0 | V |
| $UV_{DBr}$ | | | Reset level | 10.5 | — | 12.5 | V |
| $UV_{Dt}$ | | | Trip level | 10.3 | — | 12.5 | V |
| $UV_{Dr}$ | | | Reset level | 10.8 | — | 13.0 | V |
| $t_{FO}$ | Fault output pulse width | $C_{FO}$ = 22nF (Note 5) | | 1.0 | 1.8 | — | ms |
| $V_{th(on)}$ | ON threshold voltage | Applied between $U_P$, $V_P$, $W_P$-$V_{PC}$, $U_N$, $V_N$, $W_N$-$V_{NC}$ | | 2.1 | 2.3 | 2.6 | V |
| $V_{th(off)}$ | OFF threshold voltage | | | 0.8 | 1.4 | 2.1 | V |

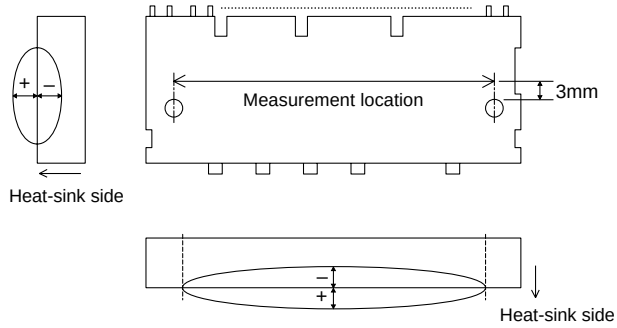
**Note 4 :** Short circuit protection is functioning only at the low-arms. Please select the value of the external shunt resistor such that the SC trip-level is less than 34 A.

**5 :** Fault signal is output when the low-arms short circuit or control supply under-voltage protective functions operate. The fault output pulse-width $t_{FO}$ depends on the capacitance value of $C_{FO}$ according to the following approximate equation : $C_{FO} = 12.2 \times 10^{-6} \times t_{FO}$ [F].

## MECHANICAL CHARACTERISTICS AND RATINGS

| Parameter | Condition | | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Mounting torque | Mounting screw : M4 | Recommended 1.18 N·m | 0.98 | — | 1.47 | N·m |
| Weight | | | — | 65 | — | g |
| Heat-sink flatness | (Note 6) | | –50 | — | 100 | μm |

**Note 6: Measurement point of heat-sink flatness**




## RECOMMENDED OPERATION CONDITIONS

| Symbol | Parameter | Condition | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{CC}$ | Supply voltage | Applied between P-N | 0 | 300 | 400 | V |
| $V_D$ | Control supply voltage | Applied between $V_{P1}$-$V_{PC}$, $V_{N1}$-$V_{NC}$ | 13.5 | 15.0 | 16.5 | V |
| $V_{DB}$ | Control supply voltage | Applied between $V_{UFB}$-$V_{UFS}$, $V_{VFB}$-$V_{VFS}$, $V_{WFB}$-$V_{WFS}$ | 13.0 | 15.0 | 18.5 | V |
| $\Delta V_D$, $\Delta V_{DB}$ | Control supply variation | | –1 | — | 1 | V/μs |
| $t_{dead}$ | Arm shoot-through blocking time | For each input signal, $T_f \leq 100°C$ | 2 | — | — | μs |
| $f_{PWM}$ | PWM input frequency | $T_f \leq 100°C$, $T_j \leq 125°C$ | — | 5 | — | kHz |
| $I_O$ | Allowable r.m.s. current | $V_{CC}$ = 300V, $V_D$ = 15V, fc = 10kHz<br>P.F = 0.8, sinusoidal<br>$T_j \leq 125°C$, $T_f \leq 100°C$ (Note 7) | — | — | 12 | Arms |
| PWIN | Minimum input pulse width | ON (Note 8) | 300 | — | — | ns |
| $V_{NC}$ | $V_{NC}$ variation | between $V_{NC}$-N (including surge) | –5.0 | — | 5.0 | V |

**Note 7 :** The allowable r.m.s. current value depends on the actual application conditions.
**8 :** The input pulse width less than PWIN might make no response.

**Fig. 4 THE DIP-IPM INTERNAL CIRCUIT**

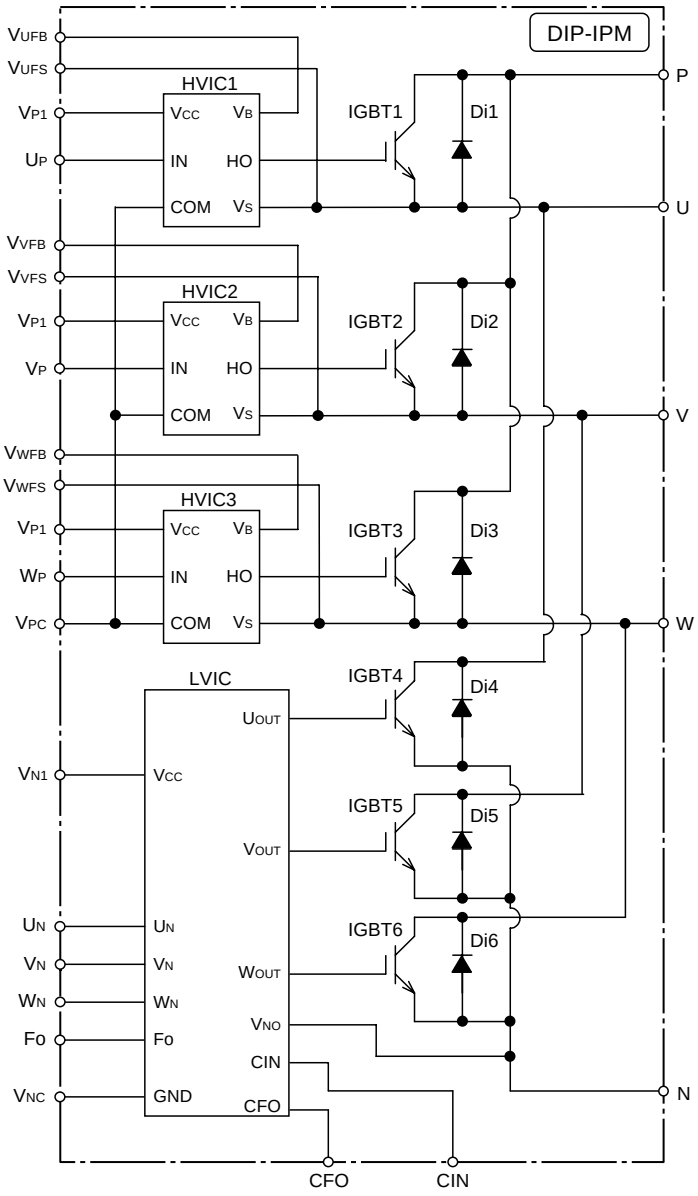
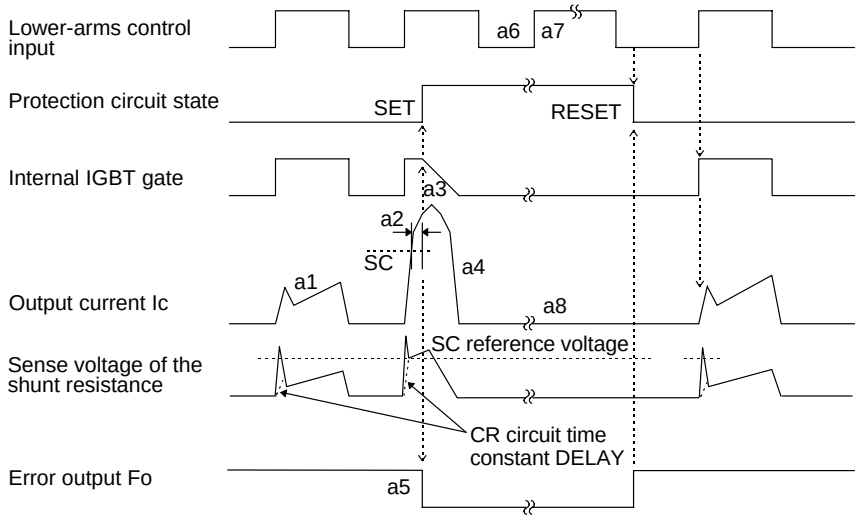


**Fig. 5 TIMING CHARTS OF THE DIP-IPM PROTECTIVE FUNCTIONS**

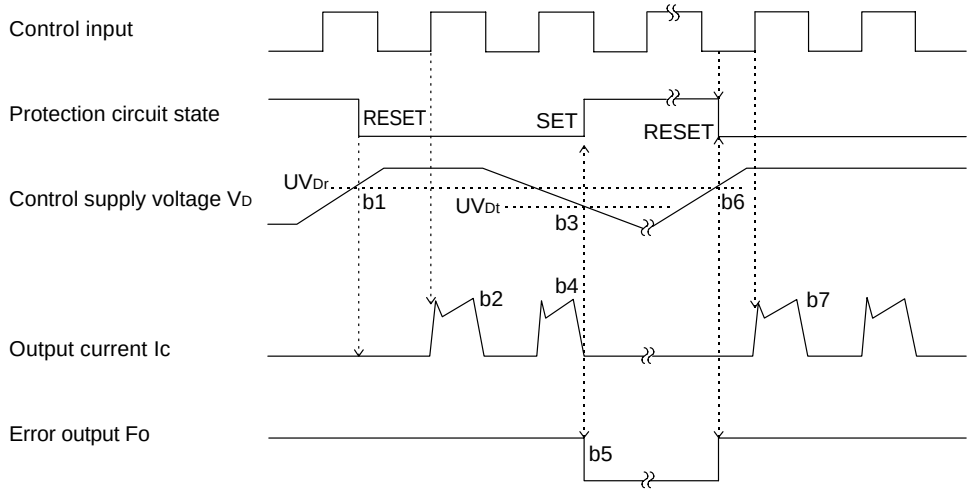
**[A] Short-Circuit Protection (Lower-arms only)**

(With the external shunt resistance and CR connection)
a1. Normal operation : IGBT ON and carrying current.
a2. Short circuit current detection (SC trigger).
a3. Hard IGBT gate interrupt.
a4. IGBT turns OFF.
a5. FO timer operation starts : The pulse width of the FO signal is set by the external capacitor CFO.
a6. Input "L" : IGBT OFF state.
a7. Input "H" : IGBT ON state, but during the FO active signal period the IGBT doesn't turn ON.
a8. IGBT OFF state.




**[B] Under-Voltage Protection (Lower-arm, UVD)**

b1. Control supply voltage rises : After the voltage level reaches UVDr, the circuits start to operate when next input is applied.
b2. Normal operation : IGBT ON and carrying current.
b3. Under voltage trip (UVDt).
b4. IGBT OFF in spite of control input condition.
b5. FO operation starts.
b6. Under voltage reset (UVDr).
b7. Normal operation : IGBT ON and carrying current.



**[C] Under-Voltage Protection (Upper-arm, $UV_{DB}$)**

c1. Control supply voltage rises : After the voltage reaches $UV_{DBr}$, the circuits start to operate when next input is applied.
c2. Normal operation : IGBT ON and carrying current.
c3. Under voltage trip ($UV_{DBt}$).
c4. IGBT OFF in spite of control input condition, but there is no $F_O$ signal output.
c5. Under voltage reset ($UV_{DBr}$).
c6. Normal operation : IGBT ON and carrying current.

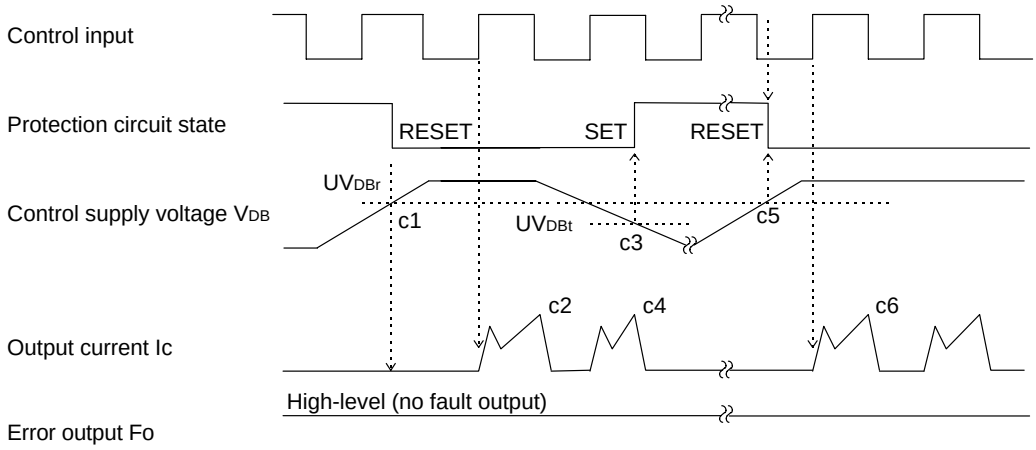
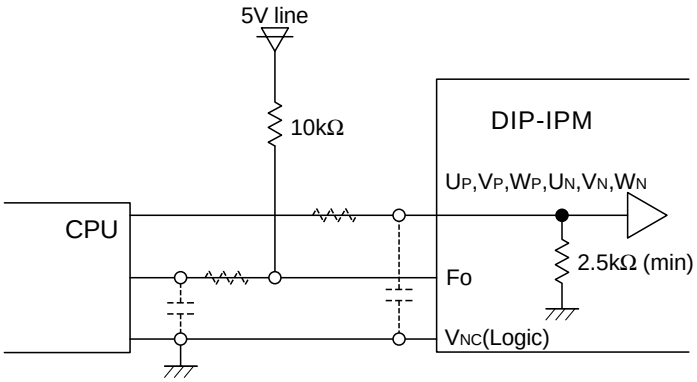



**Fig. 6 RECOMMENDED CPU I/O INTERFACE CIRCUIT**




**Note :** RC coupling at each input (parts shown dotted) may change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board.
The DIP-IPM input signal section integrates a 2.5kΩ(min) pull-down resistor. Therefore, when using a external filtering resistor, care must be taken to satisfy the turn-on threshold voltage requirement.

**Fig. 7 RECOMMENDED WIRING OF SHUNT RESISTANCE**

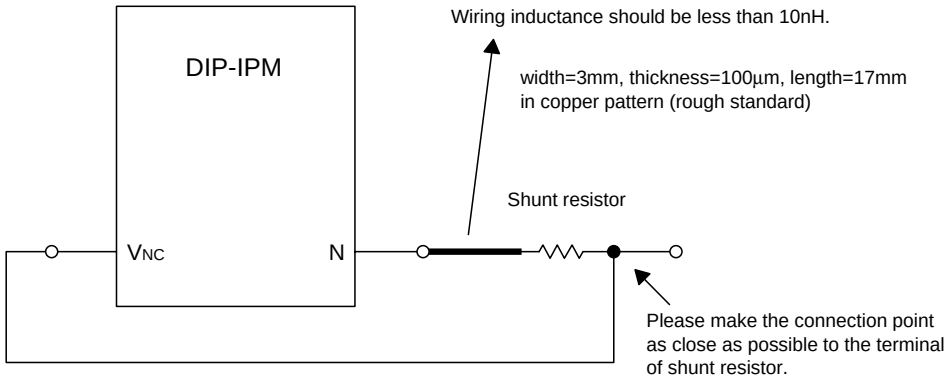
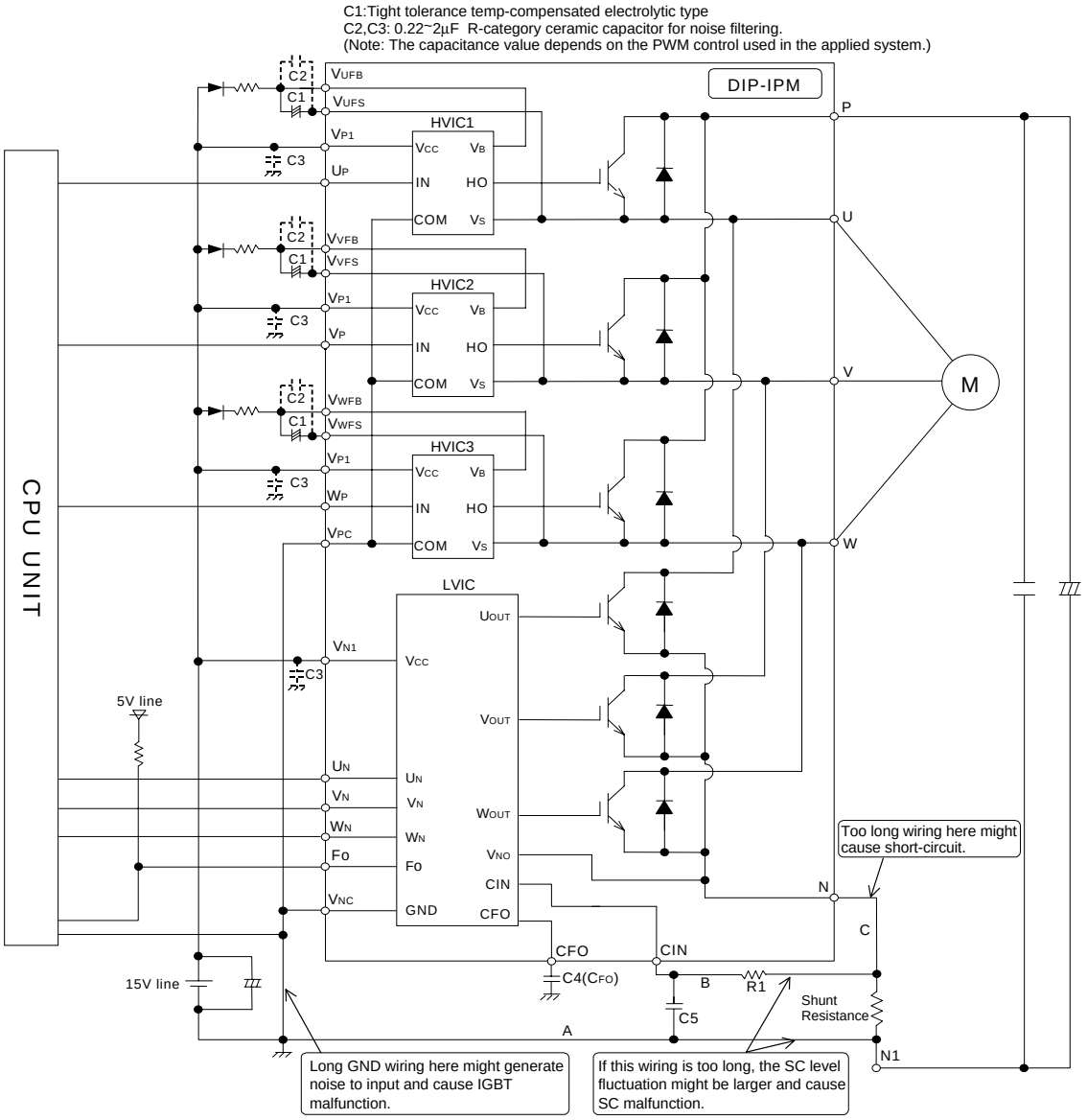


**Fig. 8 TYPICAL DIP-IPM APPLICATION CIRCUIT EXAMPLE**




**Note 1 :** To prevent the input signals oscillation, the wiring of each input should be as short as possible. (Less than 2cm)

**2 :** By virtue of integrating an application specific type HVIC inside the module, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.

**3 :** $F_O$ output is open collector type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 10kΩ resistor.

**4 :** $F_O$ output pulse width is determined by the external capacitor between CFO and $V_{NC}$ terminals ($C_{FO}$). (Example : $C_{FO}$ = 22 nF → $t_{FO}$ = 1.8 ms (typ.))

**5 :** The logic of input signal is high-active. The DIP-IPM input signal section integrates a 2.5kΩ (min) pull-down resistor. Therefore, when using external filtering resistor, care must be taken to satisfy the turn-on threshold voltage requirement.

**6 :** To prevent malfunction of protection, the wiring of A, B, C should be as short as possible.

**7 :** Please set the $R_1C_5$ time constant in the range 1.5~2µs.

**8 :** Each capacitor should be located as nearby the pins of the DIP-IPM as possible.

**9 :** To prevent surge destruction, the wiring between the smoothing capacitor and the P&N1 pins should be as short as possible. Approximately a 0.1~0.22µF snubber capacitor between the P&N1 pins is recommended.